Patent
Attorney's Docket No. 009683-362

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT
APPLICATION TRANSMITTAL LETTER

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed for filing is the utility patent application of Atsushi ISHIKAWA for IMAGE PROCESSOR CAPABLE OF REDUCING GRADATION AT HIGH SPEED.

Also enclosed are:

[X] 4 sheet(s) of [X] formal [ ] informal drawing(s);

[X] a claim for foreign priority under 35 U.S.C. §§ 119 and/or 365 is [ ] hereby made to _ filed in _ on _;

[X] in the declaration;

[ ] a certified copy of the priority document;

[ ] a General Authorization for Petitions for Extensions of Time and Payment of Fees;

[X] an Assignment document;

[ ] an Information Disclosure Statement; and

[ ] Other: _____.

[X] An [X] executed [ ] unexecuted declaration of the inventor(s)

[X] also is enclosed [ ] will follow.

[ ] Please amend the specification by inserting before the first line the sentence --This application claims priority under 35 U.S.C. §§ 119 and/or 365 to _ filed in _ on _; the entire content of which is hereby incorporated by reference.--

[ ] A bibliographic data entry sheet is enclosed.

[ ] Small entity status is hereby claimed.

[X] The filing fee has been calculated as follows [ ] and in accordance with the enclosed preliminary amendment:

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEE
Basic Application Fee					$710.00 (101)
Total Claims	18	MINUS 20 =	0	× $18.00 (103) =	0
Independent Claims	3	MINUS 3 =	0	× $80.00 (102) =	0
If multiple dependent claims are presented, add $270.00 (104)					
Total Application Fee					710.00
If small entity status is claimed, subtract 50% of Total Application Fee					
Add Assignment Recording Fee $ if Assignment document is enclosed					40.00
TOTAL APPLICATION FEE DUE					**750.00**

[ ] This application is being filed without a filing fee. Issuance of a Notice to File Missing Parts of Application is respectfully requested.

[X] A check in the amount of $ 750.00 is enclosed for the fee due.

[ ] Charge $ _____ to Deposit Account No. 02-4800 for the fee due.

[X] The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17 and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in duplicate.

Please address all correspondence concerning the present application to:

Platon N. Mandros
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: October 20, 2000

By: William C Rowland, Reg 30888, for
Platon N. Mandros
Registration No. 22,124

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

Image Processor Capable of Reducing Gradation at High Speed

This application is based on application No. 11-299437 filed in Japan, the contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an image processor, and more particularly, it relates to an image processor converting M-valued image data of a target pixel to N (M > N)-valued image data (N-arization) on the basis of error diffusion.

Description of the Related Art

An image processor utilizing error diffusion is known in general. General error diffusion is performed on the basis of the following equation.

Assuming that I_{xy} ($0 \leqq I_{xy} \leqq 1$) represents input image data of a pixel (target pixel) having coordinates (x, y) and B_{xy} (0 or 1) represents output two-valued image data (N-valued image data), two-valued error data E_{xy} is expressed as follows:

$$E_{xy} = I_{xy} - B_{xy} \quad \ldots (1)$$

According to the error diffusion, the image data I_{xy} of the target pixel is corrected with an average weighted error $EAVE_{xy}$ of two-valued errors of peripheral pixels thereof, in order to reduce the two-valued error data E_{xy} on the average. The average weighted error $EAVE_{xy}$ is obtained as follows:

$$EAVE_{xy} = \Sigma K_{xy} \times E_{ij} \quad \ldots (2)$$

In general, the weighting factor K_{ij} is increased as approaching the target pixel. As shown in Fig. 3, a filter computes the average weighted error $EAVE_{xy}$ generally with a matrix size i of five pixels along the main scanning direction of the filter and a matrix size j of two to three pixels along the subscanning direction. The weighting factor K_{ij} is increased as approaching the target pixel (denoted by "*" in Fig. 3).

Corrected image data I'_{xy} of the target pixel is expressed as follows:

$$I'_{xy} = I_{xy} + EAVE_{xy} \quad \ldots (3)$$

The obtained corrected image data I'_{xy} is binarized with a prescribed threshold Th.

$B_{xy} = 1$ (when $I'_{xy} \geqq Th$)

$B_{xy} = 0$ (when $I'_{xy} < Th$) ... (4)

The two-valued error data E_{xy} is computed from the corrected image data I'_{xy} and a reference value B'_{xy} obtained on the basis of the result of binarization (two-valued image data).

$$E_{xy} = I'_{xy} - B'_{xy} \quad \text{... (5)}$$

In general, the reference value B'_{xy} is:

$B'_{xy} = HB$ (when $B_{xy} = 1$)

$B'_{xy} = LB$ (when $B_{xy} = 0$) ... (6)

The reference values HB and LB are given by the upper limit (= 1) and the lower limit (= 0) of the dynamic range of the pixel respectively.

Fig. 4 is a block diagram showing the structure of a conventional image processor employing error diffusion.

Referring to Fig. 4, the image processor is formed by an error storage memory 1, an error computing part (product-sum operation part) 2 computing errors on the basis of an error weighting filter, an adder 3, a comparator 4, a subtracter 5 and a selector 6.

The error storage memory 1 stores two-valued errors necessary for computing the average weighted error $EAVE_{xy}$. The error storage memory 1 outputs the two-valued errors to the error computing part 2. The error computing part 2 performs a product-sum operation of the weighting factor K_{ij} and the errors for computing the average weighted error $EAVE_{xy}$ and outputting the same to the adder 3 (the processing of the above equation (2)).

The adder 3 adds the image data I_{xy} of the target pixel with the average weighted error $EAVE_{xy}$ of the peripheral pixels and computes the corrected image data I'_{xy}. Then, the adder 3 outputs the corrected image data I'_{xy} to the comparator 4 for binarization and the subtracter 5 for error computing (the processing of the above equation (3)).

The comparator 4 compares the corrected image data I'_{xy} with the prescribed threshold Th (e.g. "127") to obtain the two-valued output B_{xy} as a result and outputs the result of the comparison to the selector 6 for selecting the reference value (the processing of the above equation (4)).

The subtracter 5 subtracts the corrected image data I'_{xy} from the reference value B'_{xy} and outputs the obtained two-valued error data E_{xy} to the error storage memory 1 (the processing of the above equation (5)).

The selector 6 selects the reference value (HB or LB) for computing the two-valued error data E_{xy} from the two-valued image data B_{xy}, and outputs the selected reference value B'_{xy} to the subtracter 5.

Referring to Fig. 4, the error computing part 2 computing the average weighted error $EAVE_{xy}$ of the peripheral pixels, the adder 3 adding the average weighted error $EAVE_{xy}$ to the input image data I_{xy} and computing the corrected image data I'_{xy}, the comparator 4 comparing the corrected image data I'_{xy} with the threshold Th and computing the two-valued image data B_{xy}, the selector 6 for selecting the reference value B'_{xy} from the two-valued image data B_{xy} and the subtracter 5 computing the two-valued error data E_{xy} from the corrected image data I'_{xy} and the reference value B'_{xy} form a feedback loop of errors.

In order to binarize the image data I_{xy} of the target pixel, the average weighted error $EAVE_{xy}$ of the peripheral pixels must be operated inclusive of a two-valued error $E_{x-1,y}$ of a precedently binarized pixel. In other words, the processing of the above equations (2) to (6) must be entirely performed in a cycle processing a single pixel. If the processing in the feedback loop is performed at a slow speed, therefore, the processing speed of the overall image processor is reduced.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an image processor having a high processing speed.

In order to attain the aforementioned object, an image processor converting M-valued image data of a target pixel to N (M > N)-valued image data by error diffusion according to an aspect of the present invention comprises a correction part correcting the M-valued image data of the target pixel with an N-valued error resulting from N-arization of peripheral pixels for the target pixel and generating corrected image data, an N-arization part comparing the corrected image data with a threshold and converting the corrected image data to N-valued image data of the

target pixel and an output part outputting an N-valued error having a smaller bit number than the corrected image data by multivalued dithering on the basis of the corrected image data and the N-valued image data.

According to another aspect of the present invention, an image processor converting M-valued image data of a target pixel to N (M > N)-valued image data by error diffusion comprises a correction part correcting the M-valued image data of the target pixel with an N-valued error resulting from N-arization of peripheral pixels for the target pixel and generating corrected image data, an N-arization part comparing the corrected image data with a threshold and converting the corrected image data to N-valued image data of the target pixel and an output part outputting an N-valued error having a smaller bit number than the corrected image data on the basis of the corrected image data and the N-valued image data.

According to still another aspect of the present invention, an image processing method of converting M-valued image data of a target pixel to N (M > N)-valued image data by error diffusion comprises steps of correcting the M-valued image data of the target pixel with an N-valued error resulting from N-arization of peripheral pixels for the target pixel and generating corrected image data, comparing the corrected image data with a threshold and converting the corrected image data to N-valued image data of the target pixel and outputting an N-valued error having a smaller bit number than the corrected image data on the basis of the corrected image data and the N-valued image data.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the structure of an image processor according to a first embodiment of the present invention;

Fig. 2 is a block diagram showing the structure of an image processor according to a second embodiment of the present invention;

Fig. 3 illustrates the structure of an error weighting filter; and

Fig. 4 is a block diagram showing the structure of a conventional image processor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram showing the structure of an image processor according to a first embodiment of the present invention. The difference between this image processor and the image processor shown in Fig. 4 is now described.

According to this embodiment, a multivalued dithering part 7 is provided between an adder 3 and a subtracter 5. The multivalued dithering part 7 bit-reduces corrected image data I'_{xy} by multivalued dithering, and outputs bit-reduced corrected image data I''_{xy} to the subtracter 5.

The multivalued dithering part 7 applies dithering to lower L bits of the corrected image data I'_{xy} consisting of K bits and converts the data of the lower L bits to 1-bit data. Thus, the multivalued dithering part 7 converts the corrected image data I'_{xy} consisting of K bits to the bit-reduced corrected image data I''_{xy}.

The dithering is a pseudo-gradation method (area gradation method) expressing gradation by a set of dots similarly to the error diffusion, and hence the quantity of information per dot is reduced due to the bit reduction while the quantity of information of the original image is preserved by the set of the dots.

A selector 6 outputs one of reference values HB and LB in response to a result B_{xy} of binarization. The reference values HB and LB have the same bit number as the bit-reduced corrected image data I''_{xy}.

The subtracter 5 subtracts a reference value B'_{xy} from the bit-reduced corrected image data I''_{xy} and outputs the result as two-valued error data E_{xy}. The bit number of the two-valued error data E_{xy}, requiring a bit indicating +/–, is larger than that of the bit-reduced corrected image data I''_{xy} by 1. An error storage memory 1 stores the value of the two-valued error data E_{xy}.

An error computing part 2 employs an error weighting filter and

outputs an average weighted error $EAVE_{xy}$ with reference to the contents of the error storage memory 1. The error computing part 2 adjusts weighting factors of the error weighting filter thereby matching the bit number of the average weighted error $EAVE_{xy}$ with that of pixel data I_{xy} of a target pixel. The average weighted error $EAVE_{xy}$ is provided with the bit indicating +/–, and hence the bit number of the average weighted error $EAVE_{xy}$ is larger than that of the pixel data I_{xy} of the target pixel by 1.

More specifically, the pixel data I_{xy} of the target pixel has eight bits, the corrected image data I'_{xy} has eight bits, the two-valued image data B_{xy} has one bit, the bit-reduced corrected image data I''_{xy} has four bits, the two-valued error data E_{xy} has 1 (indicating +/–) + 4 bits, and the average weighted error $EAVE_{xy}$ has 1 (indicating +/–) + 8 bits.

According to this embodiment, as hereinabove described, the bit number of computing between the multivalued dithering part 7 and the error computing part 2 can be reduced as compared with the prior art. Thus, high-speed computing can be performed for providing an image processor having a high processing speed.

The capacity of the error storage memory 1 for storing error data can be remarkably reduced by reducing the bit number of t error data.

The sum of the weighting factors of the error weighting filter shown in Fig. 1 is $16 = 2^4$. When the multivalued dithering part 7 reduces four bits, therefore, no division (by "16" in Fig. 4, for example) is required for a product-sum operation of peripheral pixels, to result in no operation error.

Referring to Fig. 1, for example, the error computing part 2 may simply multiply the output from the error storage memory 1 by any of the numerical values "1" to "3" and add the sum, whereby a high-speed operation can be performed.

When a relation $m = 2^n$ holds between the number n of bit reduction by the multivalued dithering and the sum m of the weighting factors, no division is required.

Fig. 2 is a block diagram showing the structure of an image processor according to a second embodiment o the present invention.

While the image processor according to the first embodiment reduces

the bit number of the corrected image data I'_{xy} by multivalued dithering and thereafter computes an N-valued error, the image processor according to the second embodiment reduces the bit number of difference data E_{xy} between corrected image data I'_{xy} and a reference value based on N-valued image data by a multivalued dithering part 7. The bit number of error data can be reduced also by reducing the bit number of the two-valued error E_{xy}, whereby a load on a product-sum operation can be reduced and the speed of a feedback loop for errors can be increased.

While each of the above embodiments has been described with reference to the processing of converting multivalued image data to two-valued image data, the present invention is not restricted to this but is also applicable to image processing converting M-valued image data to N (M > N)-valued image data on the basis of error diffusion. In order to reduce the bit number, simple binarization or error diffusion may be employed in place of the multivalued dithering.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. An image processor converting M-valued image data of a target pixel to N (M > N)-valued image data by error diffusion, comprising:

correction means correcting said M-valued image data of said target pixel with an N-valued error resulting from N-arization of peripheral pixels for said target pixel and generating corrected image data;

N-arization means comparing said corrected image data with a threshold and converting said corrected image data to N-valued image data of said target pixel; and

output means outputting an N-valued error having a smaller bit number than said corrected image data by multivalued dithering on the basis of said corrected image data and said N-valued image data.

2. The image processor according to claim 1, further comprising:

storage means storing said N-valued error output from said output means.

3. The image processor according to claim 2, wherein

said correction means computes an average weighted error on the basis of said N-valued error of said peripheral pixels for said target pixel stored in said storage means and weighting factors, and performs correction on the basis of said average weighted error.

4. The image processor according to claim 3, wherein

a relation $m = 2^n$ holds between the number n of bit reduction by said multivalued dithering and the sum m of said weighting factors.

5. The image processor according to claim 1, wherein

said output means includes means performing multivalued dithering on said corrected image data.

6. The image processor according to claim 5, wherein

said output means generates said N-valued error on the basis of said corrected image data subjected to said multivalued dithering and said n-valued image data.

7. The image processor according to claim 1, wherein

said output means includes means performing multivalued dithering on difference data between said corrected image data and data based on said N-valued image data.

8. An image processor converting M-valued image data of a target pixel to N (M > N)-valued image data by error diffusion, comprising:

correction means correcting said M-valued image data of said target pixel with an N-valued error resulting from N-arization of peripheral pixels for said target pixel and generating corrected image data;

N-arization means comparing said corrected image data with a threshold and converting said corrected image data to N-valued image data of said target pixel; and

output means outputting an N-valued error having a smaller bit number than said corrected image data on the basis of said corrected image data and said N-valued image data.

9. The image processor according to claim 8, further comprising:

storage means storing said N-valued error output from said output means.

10. The image processor according to claim 9, wherein

said correction means computes an average weighted error on the basis of said N-valued error of said peripheral pixels for said target pixel stored in said storage means and weighting factors, and performs correction on the basis of said average weighted error.

11. The image processor according to claim 8, wherein

said output means includes means performing multivalued dithering

on said corrected image data.

12. The image processor according to claim 11, wherein

said output means generates said N-valued error on the basis of said corrected image data subjected to said multivalued dithering and said N-valued image data.

13. The image processor according to claim 8, wherein

said output means includes means performing multivalued dithering on difference data between said corrected image data and data based on said N-valued image data.

14. An image processing method of converting M-valued image data of a target pixel to N (M > N)-valued image data by error diffusion, comprising steps of:

correcting said M-valued image data of said target pixel with an N-valued error resulting from N-arization of peripheral pixels for said target pixel and generating corrected image data;

comparing said corrected image data with a threshold and converting said corrected image data to N-valued image data of said target pixel; and

outputting an N-valued error having a smaller bit number than said corrected image data on the basis of said corrected image data and said N-valued image data.

15. The image processing method according to claim 14, further including:

a step of computing an average weighted error on the basis of said N-valued error of said peripheral pixels for said target pixel and weighting factors,

for generating said corrected image data on the basis of said average weighted error.

16. The image processing method according to claim 14, further

including:

a step of performing multivalued dithering on said corrected image data.

17. The image processing method according to claim 16, wherein said N-valued error is generated on the basis of said corrected image data subjected to said multivalued dithering and said N-valued image data.

18. The image processing method according to claim 14, further including:

a step of performing multivalued dithering on difference data between said corrected image data and data based on said N-valued image data.

ABSTRACT OF THE DISCLOSURE

An image processor employing error diffusion is provided with a multivalued dithering part, for reducing the bit number of computing in a feedback loop for errors. Thus, an operation can be performed at a high speed while the capacity of an error storage memory can be reduced.

FIG. 1

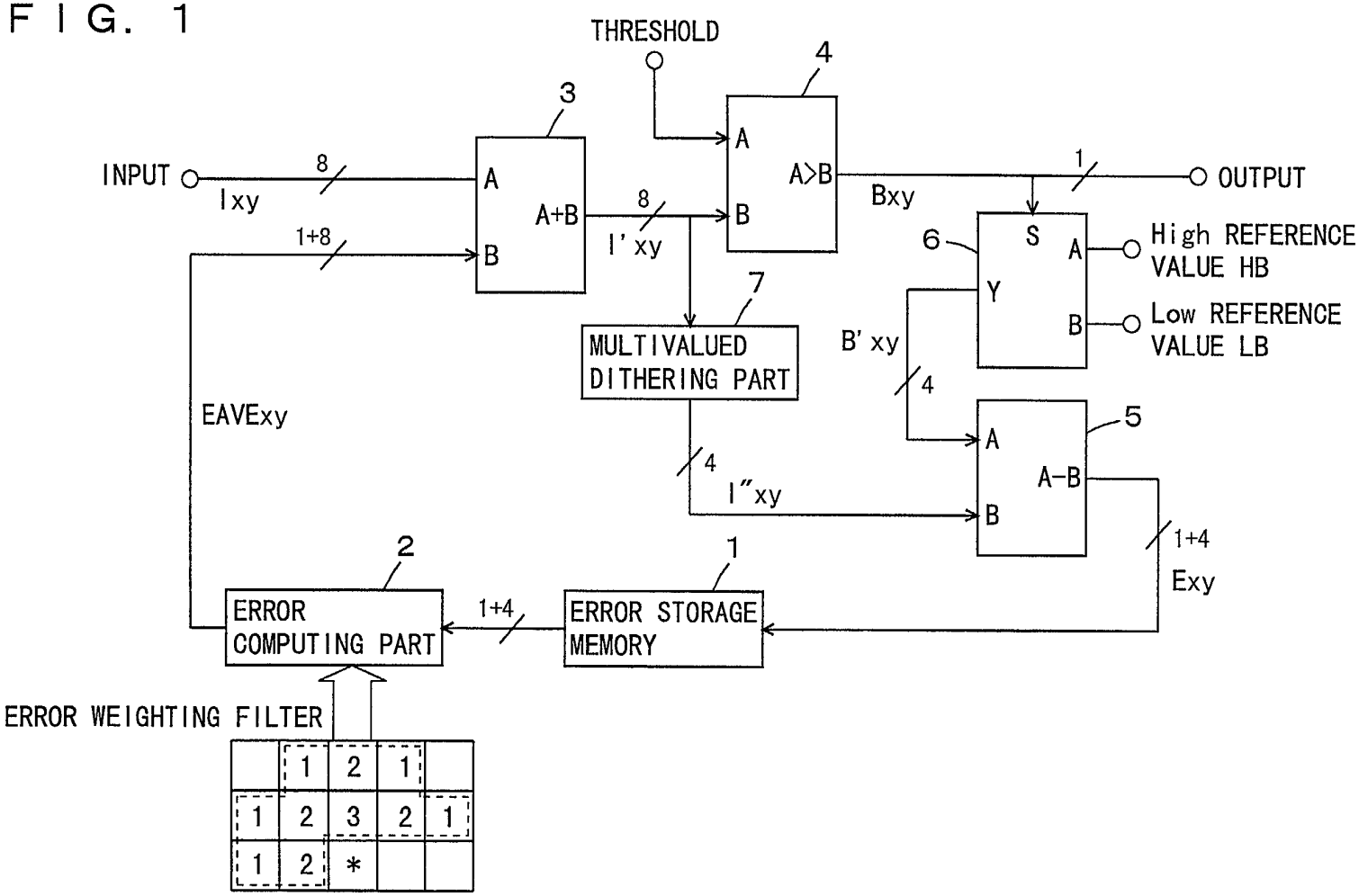

THRESHOLD
4
3
INPUT
8
Ixy
A
A+B
B
A
A>B
B
1
OUTPUT
Bxy
8
I'xy
1+8
6
S
A
Y
B
High REFERENCE VALUE HB
Low REFERENCE VALUE LB
7
MULTIVALUED DITHERING PART
B'xy
4
EAVExy
5
A
A-B
B
4
I"xy
1+4
Exy
2
1
ERROR COMPUTING PART
1+4
ERROR STORAGE MEMORY
ERROR WEIGHTING FILTER
1 2 1
1 2 3 2 1
1 2 *

FIG. 2

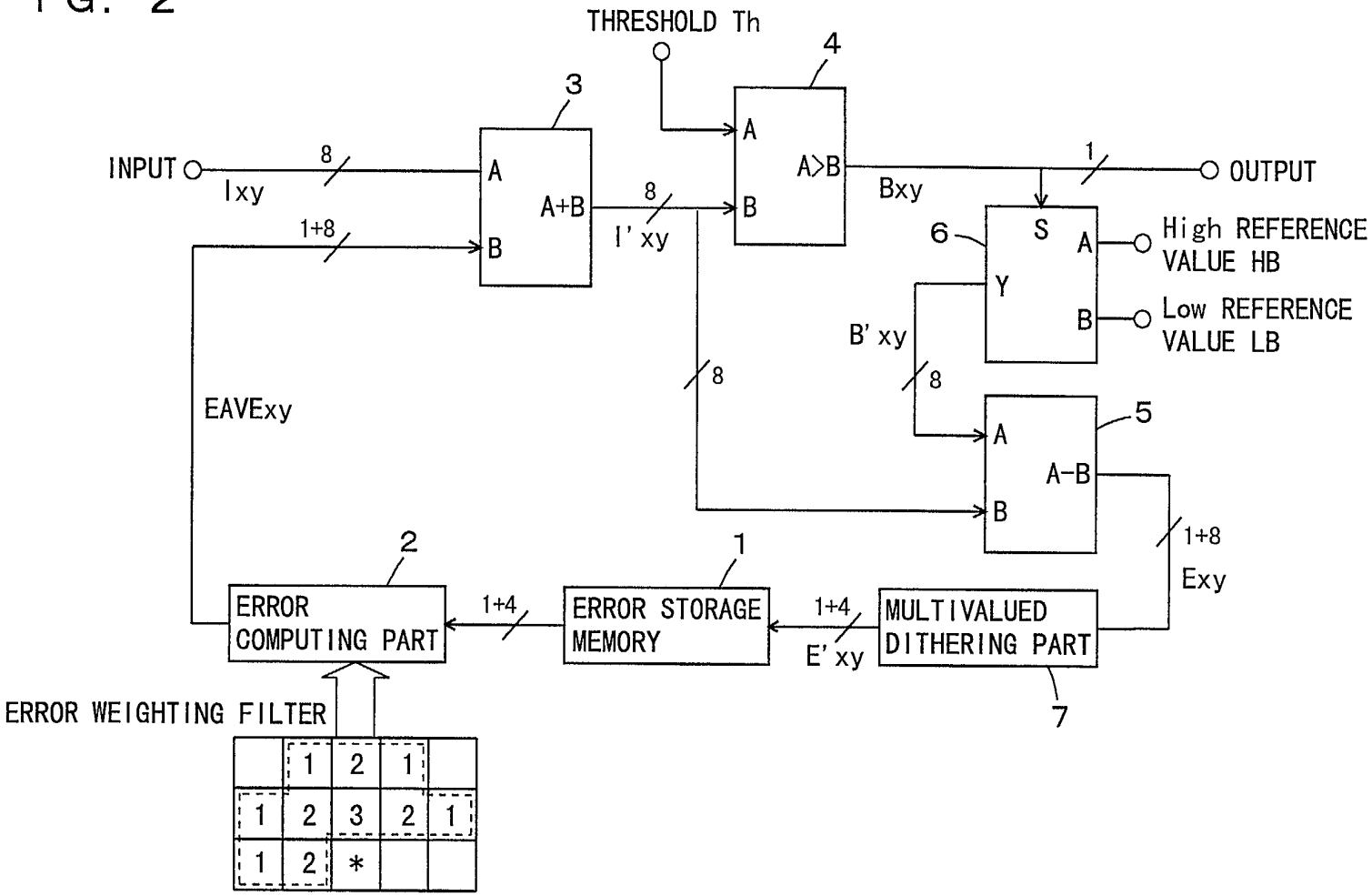

THRESHOLD Th
4
3
INPUT
8
Ixy
A
A+B
B
8
I'xy
A
A>B
B
1
Bxy
OUTPUT
1+8
6
S
A
Y
B
High REFERENCE VALUE HB
Low REFERENCE VALUE LB
B'xy
8
8
EAVExy
A
A-B
B
5
1+8
Exy
2
1
ERROR COMPUTING PART
1+4
ERROR STORAGE MEMORY
1+4
E'xy
MULTIVALUED DITHERING PART
7
ERROR WEIGHTING FILTER
1 2 1
1 2 3 2 1
1 2 *

FIG. 3

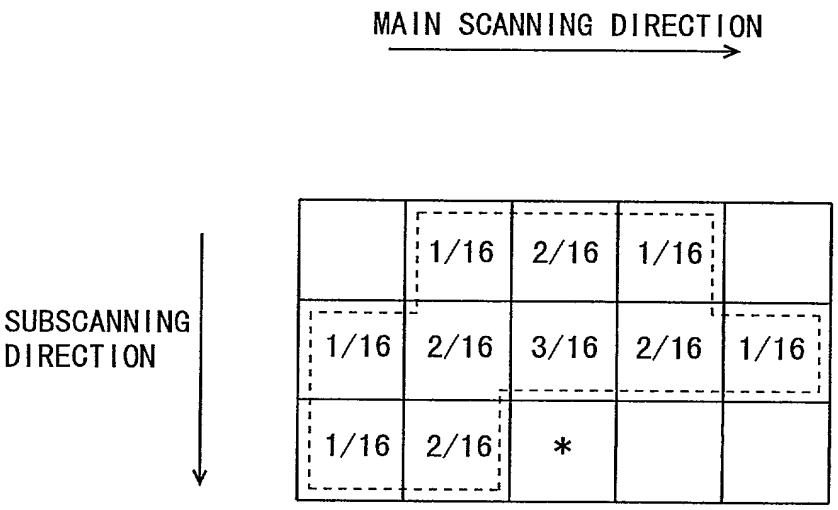
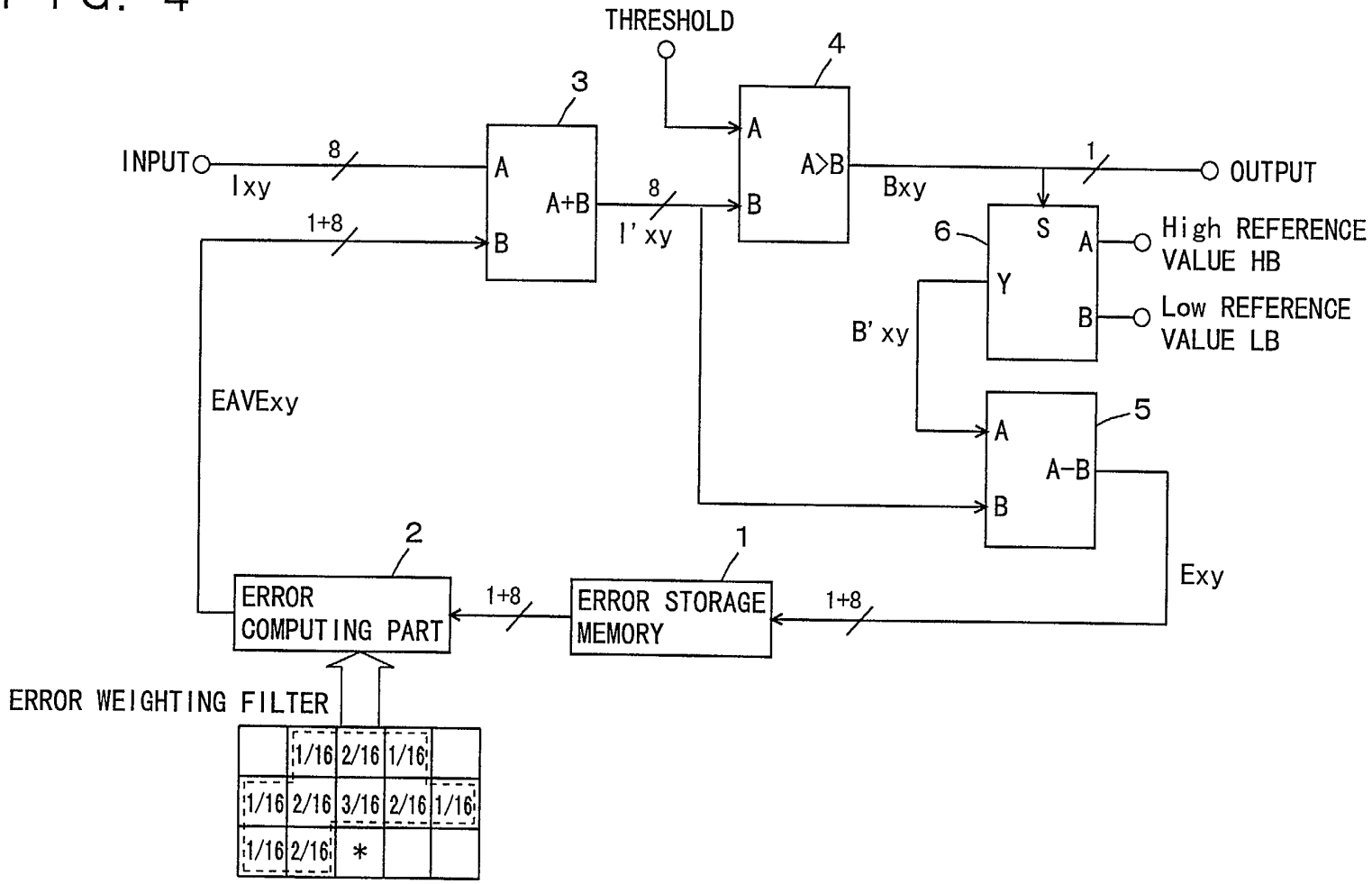

MAIN SCANNING DIRECTION
SUBSCANNING DIRECTION
1/16
2/16
1/16
1/16
2/16
3/16
2/16
1/16
1/16
2/16
*

FIG. 4


THRESHOLD
4
3
INPUT
8
Ixy
A
A+B
B
8
I'xy
A
A>B
B
1
Bxy
OUTPUT
1+8
6
S
A
Y
B
High REFERENCE VALUE HB
Low REFERENCE VALUE LB
B'xy
EAVExy
5
A
A-B
B
2
1
ERROR COMPUTING PART
1+8
ERROR STORAGE MEMORY
1+8
Exy
ERROR WEIGHTING FILTER
1/16 2/16 1/16
1/16 2/16 3/16 2/16 1/16
1/16 2/16 *

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No.

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

IMAGE PROCESSOR CAPABLE OF REDUCING GRADATION AT HIGH SPEED

the specification of which

(check one) ☒ is attached hereto;

☐ was filed on _____ as

Application No. _____

and was amended on _____; (if applicable)

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

COMBINED DECLARATION AND POWER OF ATTORNEY	Attorney's Docket No.

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
Japan	11-299437(P)	21/Oct./1999	YESX NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

William L. Mathis	17,337	R. Danny Huntington	27,903	Gerald F. Swiss	30,113
Robert S. Swecker	19,885	Eric H. Weisblatt	30,505	Michael J. Ure	33,089
Platon N. Mandros	22,124	James W. Peterson	26,057	Charles F. Wieland III	33,096
Benton S. Duffett, Jr.	22,030	Teresa Stanek Rea	30,427	Bruce T. Wieder	33,815
Norman H. Stepno	22,716	Robert E. Krebs	25,885	Todd R. Walters	34,040
Ronald L. Grudziecki	24,970	William C. Rowland	30,888	Ronni S. Jillions	31,979
Frederick G. Michaud, Jr.	26,003	T. Gene Dillahunty	25,423	Harold R. Brown III	36,341
Alan E. Kopecki	25,813	Patrick C. Keane	32,858	Allen R. Baum	36,086
Regis E. Slutter	26,999	Bruce J. Boggs, Jr.	32,344	Steven M. du Bois	35,023
Samuel C. Miller, III	27,360	William H. Benz	25,952	Brian P. O'Shaughnessy	32,747
Robert G. Mukai	28,531	Peter K. Skiff	31,917	Kenneth B. Leffler	36,075
George A. Hovanec, Jr.	28,223	Richard J. McGrath	29,195	Fred W. Hathaway	32,236
James A. LaBarre	28,632	Matthew L. Schneider	32,814		
E. Joseph Gess	28,510	Michael G. Savage	32,596		

21839

and: _____

Address all correspondence to:

21839

Platon N. Mandros
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404

Address all telephone calls to: Platon N. Mandros at (703) 836-6620.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	SIGNATURE	DATE
Atsushi ISHIKAWA	Atsushi Ishikawa	Oct. 5, 2000
RESIDENCE	CITIZENSHIP	
Anjyo-Shi, Aichi-Ken, Japan	Japanese	
POST OFFICE ADDRESS c/o MINOLTA CO.,LTD., Osaka Kokusai Bldg.,3-13, 2-Chome,Azuchi-Machi,Chuo-Ku,Osaka-Shi,Osaka,541-8556 Japan		
FULL NAME OF SECOND JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		

(1/00)